## REMARKS

Concurrently filed herewith is a Petition for Extension of Time and fee for three month's time extension.

Claims 1-35 are all the claims presently pending in this application.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 19-23 are allowed.

Claim 24, 26, 28, 29, and 31 are understood as standing rejected under 35 U.S.C. §102(e) as being anticipated by Levy (U.S. Patent No. 5,923,892). Claims 1, 2, 4-16, and 18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Levy, further in view of Holmbo (U.S. Patent No. 4,860,200). Claim 3 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Levy/Holmbo, further in view of Irwin (U.S. Patent No. 4,695,945). Claim 17 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Levy/Holmbo, further in view of Yamanaka (U.S. Patent No. 4,774,625). Claims 33 and 35 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Levy, further in view of Yamanaka.

These rejections are respectfully traversed in the following discussion.

## I. THE CLAIMED INVENTION

As described in, for example new claim 24, the claimed invention is directed to a microprocessor system for executing instructions described in a program. A main processor executes by means of hardware those instructions which belong to a first instruction set and executes by means of software those instructions which belong to a second instruction set.

A co-processor is operative under the control of the main processor for autonomously fetching an instruction belonging to the second instruction set to execute the fetched instruction by means of hardware of the co-processor. The coprocessor is provided with a stack memory for holding data generated in the course of execution of an instruction which belongs to the second instruction set, a stack pointer for holding an address of the most recent

data in the stack memory, a program counter for holding an address of an instruction which is currently processed and belongs to the second instruction set, and an updating circuit for, in response to the detection of an encounter with a specific instruction among instructions belonging to the second instruction set for which data presently under the control of the main processor needs to be handled, issuing a notification of the encounter to the main processor to request the main processor to execute the specific instruction, and for updating the stack pointer in the stack memory and the program counter in the coprocessor during an execution by the main processor.

In contrast, in conventional computer architecture, the main processor takes over the complete execution of the commands, including the updating of its own stack memory and program pointer. The present invention, therefore, reduces the processing load of the main processor when the main processor is executing the instructions sent over by the coprocessor.

## II. THE PRIOR ART REJECTIONS

A co-processor according to the present invention is provided with an updating circuit which, in response to the detection of an encounter with a specific instruction among instructions belonging to a second instruction set for which data presently under the control of a main processor needs to be handled, issues a notification of the encounter to the main processor to thereby request the main processor to execute the specific instruction, and updates a stack pointer in a stack memory and a program counter.

Employing such a structure makes it possible to execute a specific set of instructions, that is, the second instruction set, at a high speed while limiting an increase of the circuitry size. In addition, software executed by the main processor can be used effectively, and the size of the hardware of the co-processor is maintained as small as possible.

In contrast, *Levy* fails to disclose or suggest the structure of the present invention described above. *Levy* discloses that a host processor 22 executes an instruction in response to a request from a coprocessor 38 (column 6, line 6, through column 7, line 5). However, *Levy* merely discloses Java instructions such as array allocation operations as a condition for the coprocessor requesting the host processor to execute an instruction (column 6, last paragraph).

The co-processor according to the present invention determines whether the co-processor can execute a fetched instruction in an unassisted manner. When the co-processor encounters an instruction that cannot be executed by the co-processor itself, this instruction is executed by software running on the main processor, and the updating process of the values of the program counter and the stack pointer accompanying with the execution of this instruction is executed by the hardware of the co-processor. As a result, it is not necessary for the main processor to update the values of the program counter and the stack pointer while the software running on the main processor is executing an instruction requested from the co-processor. Therefore, a beneficial effect is obtained that the processing load on the software running on the main processor can be decreased.

Applicant submits that the prior art of record makes no suggestion for this combination of computer architecture.

The Rejection for Claims 24, 26, 28, 29, and 31

In paragraphs 5-8, the Examiner alleges that Levy anticipates the present invention as described in claims 24, 26, 28, 29, and 31. Applicant respectfully disagrees.

The rejection currently of record suggests that the Examiner considers that the wording of independent claim 24 does not convey this distinct advantage of the present invention. Therefore, Applicant has amended claim 24 to clarify that the updating of the program counter and stack pointer by the co-processor updating circuit occurs when the *main processor is executing one of the second instruction set instructions* that the co-processor is not designed to execute.

Levy clearly fails to teach or suggest this aspect of the present invention, since the main processor simply takes over execution of the second instruction set instruction and there is no need to have the co-processor attempt to maintain its program counter and stack pointer to correspond with the execution of that instruction. Therefore, whatever similarities may exist between Levy and the present invention, this aspect of updating the counter and pointer in the co-processor even thought the main processor is actually executing the instruction is clearly counter intuitive and, therefore, distinctive of the present invention.

An advantage of this aspect of the present invention is that the processing load of the main processor is reduced.

Hence, turning to the clear language of the claims, in Levy there is no teaching or

suggestion of: "... an updating circuit for, in response to the detection of an encounter with a specific instruction among instructions belonging to said second instruction set for which data presently under the control of said main processor needs to be handled, issuing a notification of said encounter to said main processor to request the main processor to execute said specific instruction, and for updating said stack pointer in said stack memory in said coprocessor and said program counter *in said coprocessor during an execution by said main processor* .....", as required by claim 24.

The Examiner relies upon Holmbo for allegedly demonstrating an interrupt encode/decode mechanism, upon Irwin for allegedly demonstrating the mechanism of detecting when the co-processor cannot itself execute an encountered instruction, and upon Yamanaka for allegedly demonstrating a plurality of co-processors. Regardless of the propriety of modifying primary reference Levy in accordance with any of these secondary references, these references fail to overcome the basic deficiency in Levy, wherein the co-processor stack pointer and program counter are updated when the main processor is executing one of the instructions that the co-processor cannot execute.

Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw this rejection based on Levy.

The Rejection for Claims 1, 2, 4-16, 18, 25, 27, 30, and 32

In paragraphs 10-27 of the Office Action, the Examiner also alleges that Levy, when modified by Holmbo, renders obvious the invention described by claims 1, 2, 4-16, 18, 25, 27, 30, and 32. Applicant submits that one of ordinary skill in the art would not agree that this evaluation is reasonable, since Holmbo is not properly combinable with Levy and, even if combined, would not provide the invention described by the claims.

In paragraph 12, the Examiner concedes that Levy fails to teach or suggest using an interrupt encoder and decoder described in independent claim 1. To overcome this deficiency, the Examiner relies upon Holmbo and alleges in paragraph 14 that Holmbo teaches using "vector interrupts" and "... that using such vector interrupts decreases the delay caused by executing an interrupt." The Examiner also alleges that one of ordinary skill in the art would have been motivated to modify Levy to incorporate an interrupt encoder and decoder in order to increase speed and efficiency.

In response, Applicant submits that the rejection currently of record is, at best, somewhat confused. First, it is noted that the rejection mysteriously switches from interrupt encoder/decoder terminology to "vector interrupts" and that these two concepts are not equivalent.

Second, it is noted that Levy already teaches something somewhat similar to vector interrupts, as is clear from the description beginning at line 60 of column 6. That is, upon reaching an instruction that the co-processor is unable to execute, the control unit 52 triggers an exception signal to notify the host processor to perform the execution.

As described at lines 22-28 of column 10, the main processor in Levy retrieves the current operational state of the co-processor via the expansion bus and, using this retrieved state information, executes the exception instruction once it has determined that the co-processor has made a request, by checking the instruction trap flag. As clearly explained at lines 55-60 of column 7 and at lines 51-59 of column 9, the instruction trap flag is used in Levy to signal to the host processor when it is expected to provide the computations not possible by the co-processor.

As explained beginning at line 5 of page 26 of the specification, by using the interrupt vector concept with an encoder/decoder, the present invention exemplarily can eliminate up to ten of the forty operation clocks conventionally required for software implementation of an instruction.

Applicant submits that the significance of the description in claim 1 is not that Levy fails to utilize interrupt vectors, but rather that the present invention uses an encoder and decoder mechanism for these interrupts. The advantage of this mechanism is that it permits the main processor to be able to immediately recognize the interrupt without having to take time to search memory for an interpretation of which set of instructions the co-processor to requesting the main processor to execute, thereby eliminating the preliminary time lost in getting the interrupt process executed by the main processor.

Third, Applicant submits that the Examiner's description of Holmbo is a bit of a mis-characterization, since the mechanism in this secondary reference does not encode the vector interrupt information, as is clear from the description at lines 42-46 of column 1 and lines 64-68 of column 3.

Rather, Holmbo addresses the entirely different problem of providing the correct protocol needed by the Z80 processor. Holmbo provides this protocol by using the latch 12 and controller 14 shown in Figure 1. The vector interrupt remains on data bus 4, as described in lines 64-68 of column 3. That is, there is no encoding of this vector interrupt itself, contrary to the Examiner's characterization.

It is noted that Levy does not indicate any incompatibility with interrupt protocols, thereby rendering as clearly unreasonable a motivation to modify Levy to incorporate a mechanism that has no useful purpose in Levy.

Moreover, as discussed above, even if the interrupt protocol conversion of Holmbo were to be incorporated into Levy, the plain meaning of the claim language of independent claim 1 would not be satisfied, since there would still be no encoder for the vector interrupt information itself.

In contrast, the present invention actually does use an encoder and decoder mechanism for its implementation of vector interrupts. This mechanism allows frequently-used interrupts to be quickly identified and implemented by the main processor.

Hence, turning to the clear language of the claims, in Levy and/or Holmbo, there is no teaching or suggestion of: "... said main processor including an interrupt request reception circuit to decode an interrupt vector ... said co-processor including an interrupt request generation circuit for encoding said interrupt vector ....", as required by claim 1.

The Examiner relies upon Irwin for allegedly demonstrating the mechanism of detecting when the co-processor cannot itself execute an encountered instruction, and upon Yamanaka for allegedly demonstrating a plurality of co-processors. But neither of these other secondary references overcomes the deficiency identified above for Levy/Holmbo.

Therefore the present invention defined by claim 1 is clearly patentable over Levy and Holmbo, the Examiner is respectfully requested to reconsider and withdraw this rejection based on these two references.

The Rejection for Claims 3, 17, and 33-35

Since the present invention is clearly patentable over Levy, Applicant declines at this time to comment on the propriety of additionally modifying Levy in accordance with Irwin and/or Yamanaka, except that comments from the previous Amendment would still apply.

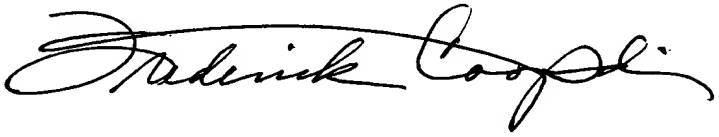
## III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-35, all the claims presently pending in the application, are patentably distinct over the prior art of record and that the application is in condition for allowance. The Examiner is respectfully requested to pass the application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,



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